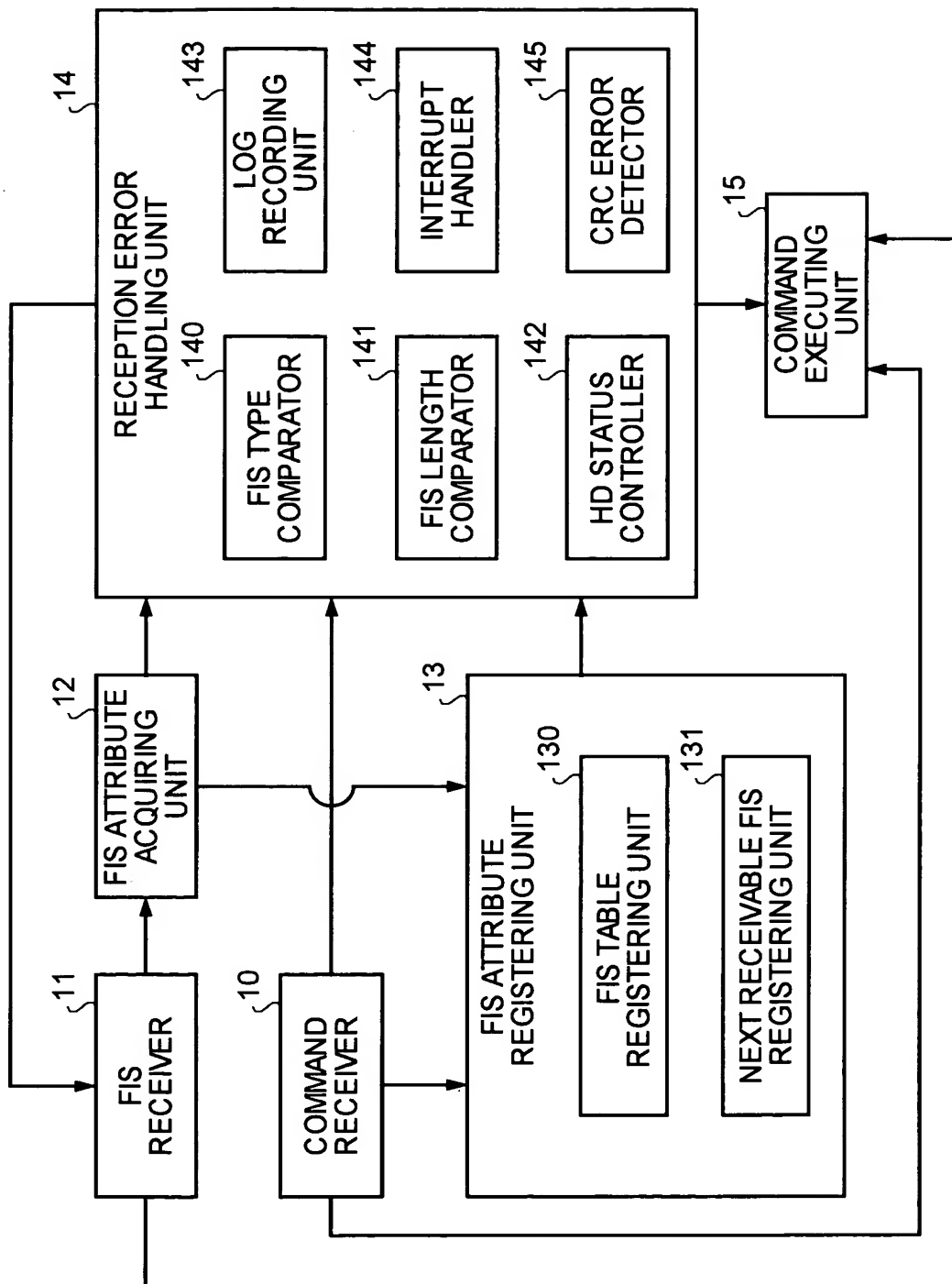


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FIG.1



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FIG.2

FIS TABLE REGISTER

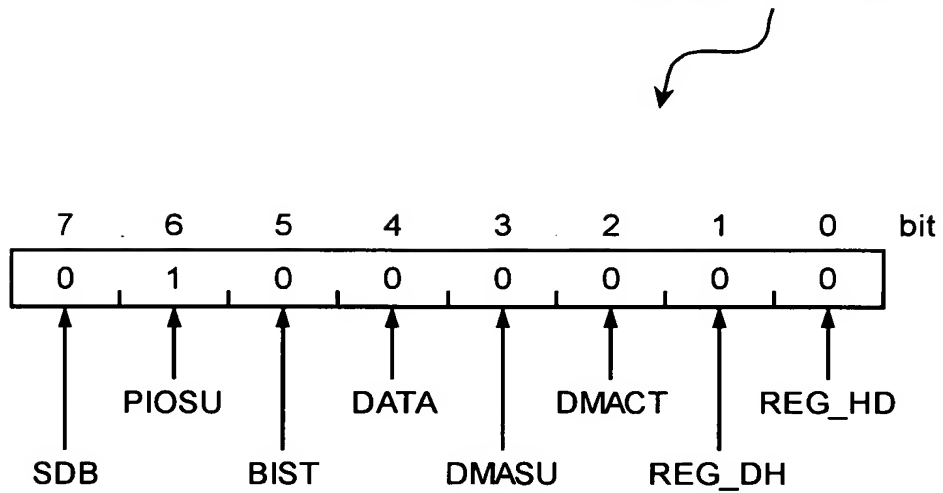
	11	10	9	8	7	6	5	4	3	2	1	0	bit
REG_HD	1	0	0	0	0	0	0	0	0	1	0	1	↓
REG_DH	1	0	0	0	0	0	0	0	0	1	0	1	↓
DMACT	0	0	0	0	0	0	0	0	0	0	0	0	↓
DMA SU	0	0	0	0	0	0	0	0	0	0	0	0	↓
DATA	1	0	0	0	1	0	0	0	0	0	0	0	↓
BIST	0	0	0	0	0	0	0	0	0	0	0	0	↓
PIOSU	1	0	0	0	0	0	0	0	0	1	0	1	↓
SDB	0	0	0	0	0	0	0	0	0	0	0	0	↓

enable bit

LENGTH OF FIS

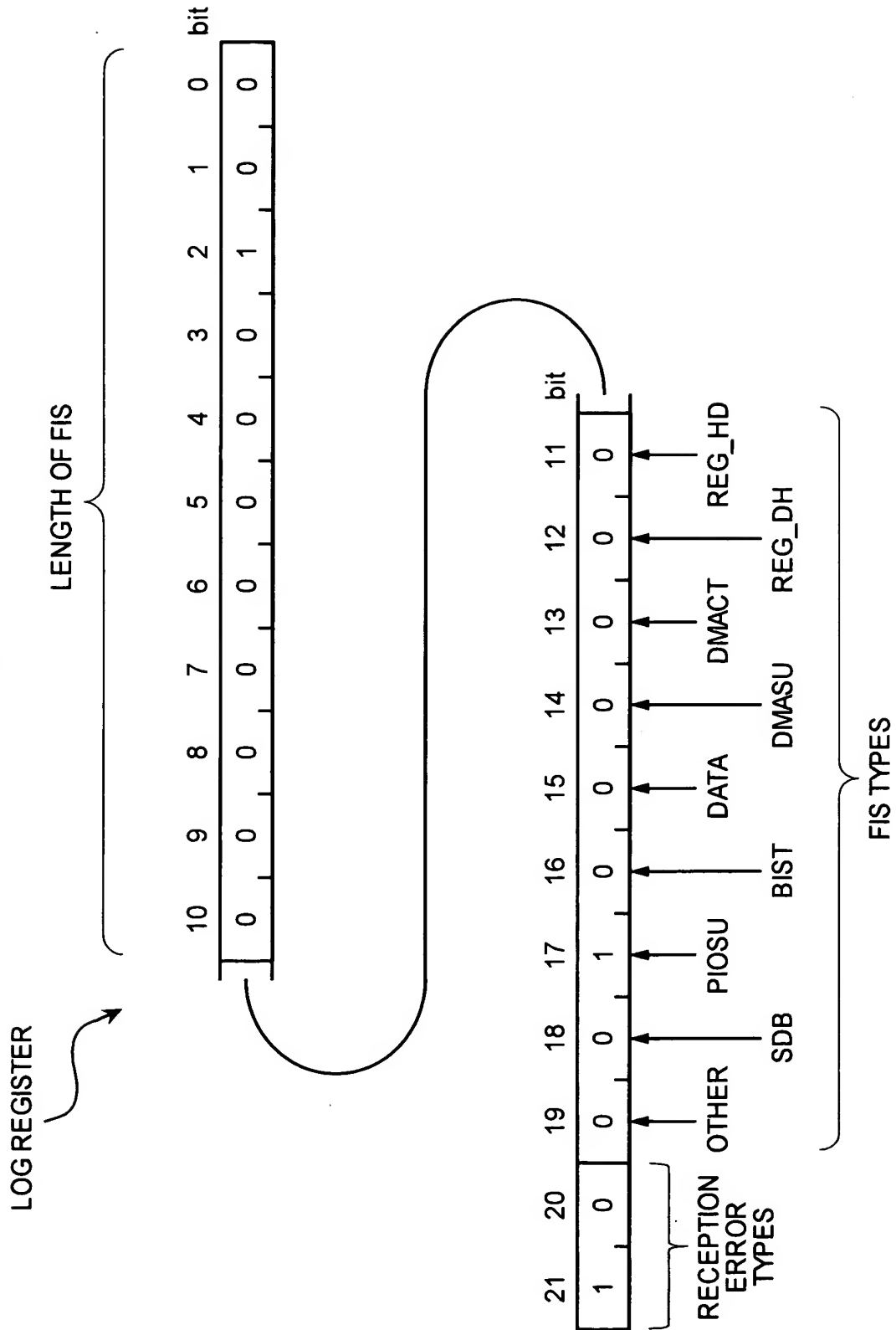
FIG.3

receivable FIS REGISTER



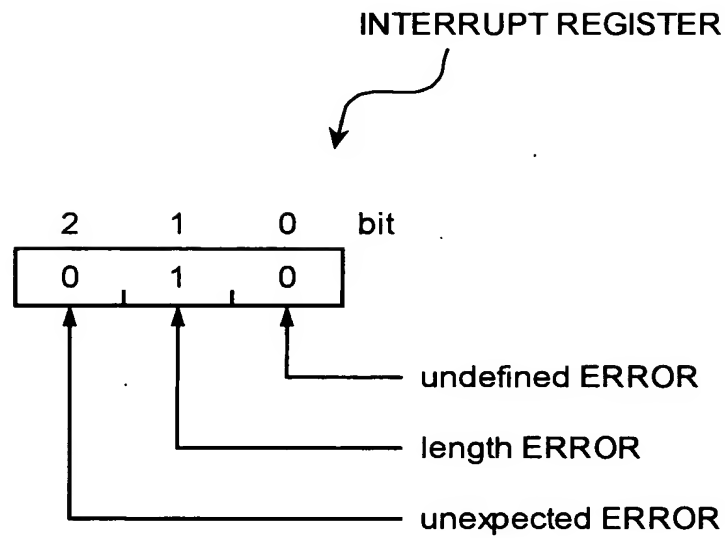
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FIG.4



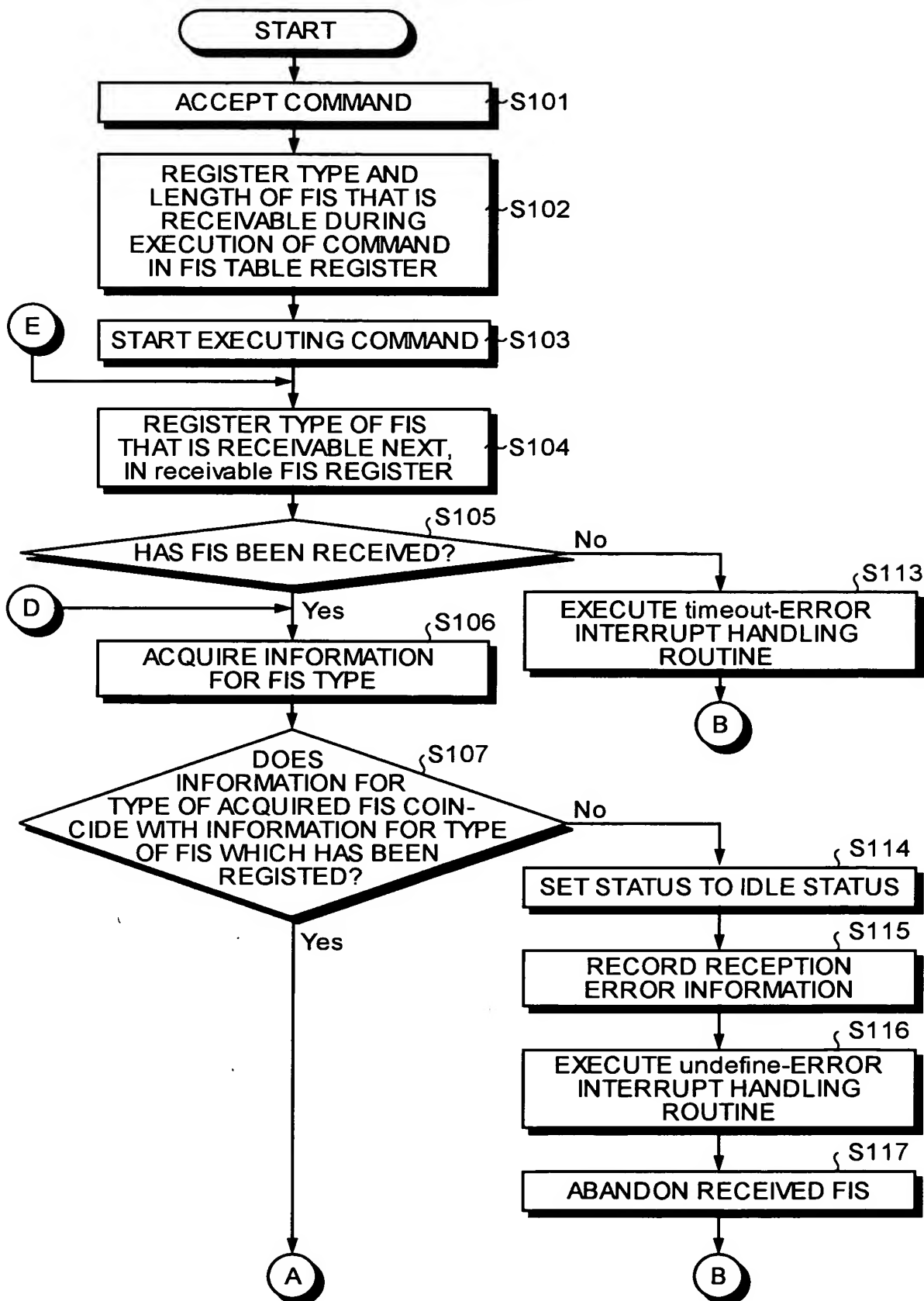
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FIG.5

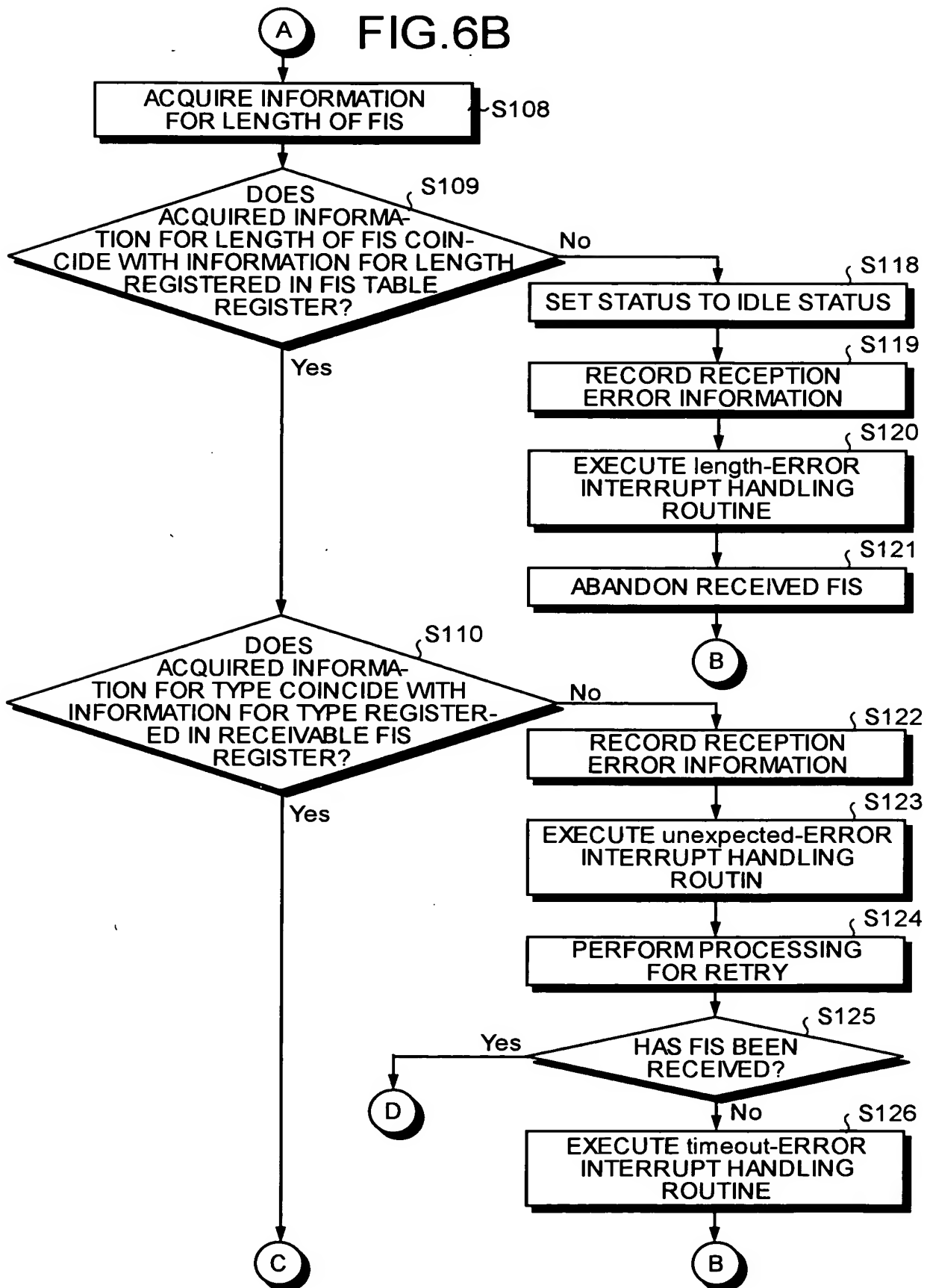


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FIG.6A



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FIG.6C

